

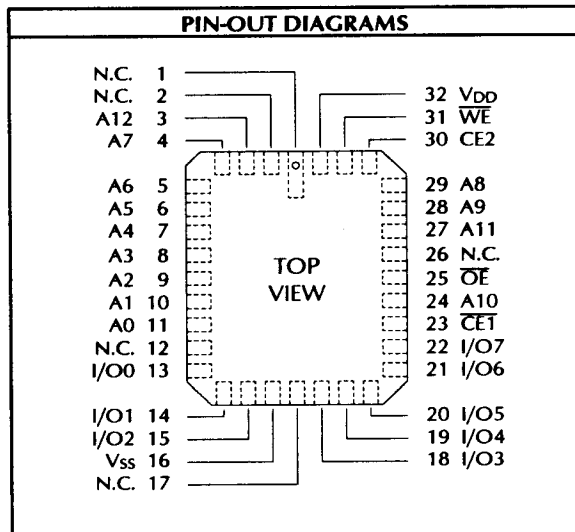
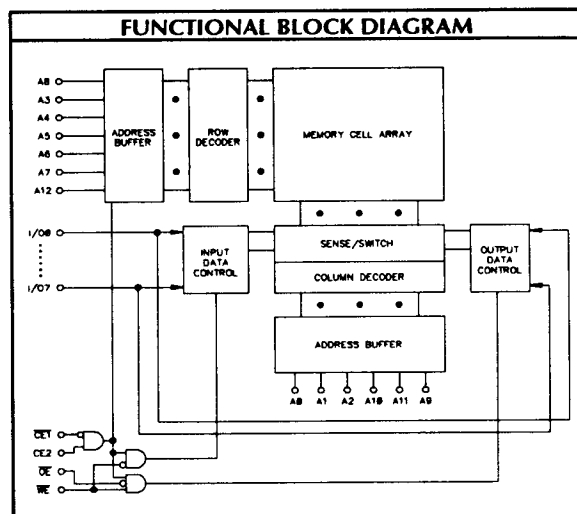
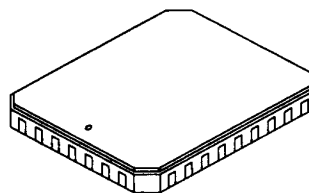
DESCRIPTION:

The DPS9264G-90, -100, -120, -150 is a 8K X 8 Static Random Access Memory (SRAM) fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The DPS9264G is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

FEATURES:

- 8,192 Words by 8-Bits Organization
- Access Times: 90, 100, 120, 150ns (max.)
- Low Power: 1.5mW (max.) Full Standby
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, ±10% Tolerance
- Three State Output
- Standard JEDEC 32-Pad LCC Package



PIN NAMES	
A0-A12	Address Inputs
I/O0-I/O7	Data Input/Output
CE1, CE2	Chip Enables
WE	Write Enable
OE	Output Enable
V _{DD}	Power (+5V)
V _{SS}	Ground
N.C.	No Connect

TRUTH TABLE						
Mode	CE1	CE2	OE	WE	I/O	I _{CC}
Not Selected	H	X	X	X	HIGH-Z	Standby
Not Selected	X	L	X	X	HIGH-Z	Standby
DOUT Disable	L	H	H	H	HIGH-Z	Active
Read	L	H	L	H	DOUT	Active
Write	L	H	X	L	D _{IN}	Active

L = LOW H = HIGH X = Don't Care

RECOMMENDED OPERATING RANGE ¹					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.3	V
V _{IL}	Input LOW Voltage	-0.3 ²		0.8	V

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-65 to + 150	°C
T _{BIAS}	Temperature Under Bias	-55 to + 125	°C
V _{DD}	Supply Voltage ¹	-0.5 to + 7.0	V
V _{I/O}	Input/Output Voltage ¹	-0.3 ² to V _{DD} +0.5	V

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{CE}	Chip Enable	7	pF	V _{IN} = 0V
C _{ADR}	Address Input	7		
C _{WE}	Write Enable	7		
C _{OE}	Output Enable	7		
C _{I/O}	Data Input/Output	10		

DC OPERATING CHARACTERISTICS: Over the operating ranges.									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{I/O} = 0V to V _{DD}	-2	2	-2	2	-2	2	µA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE1 and OE = V _{IH} , CE2 and WE = V _{IL}	-2	2	-2	2	-2	2	µA
I _{CC1}	Operating Supply Current	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	-	40	-	45	-	50	mA
I _{CC2}	Average Operating Supply Current	V _{IN} = V _{IL} or V _{IH} , I _{OUT} = 0mA, t _{CYC} = min.	-	60	-	65	-	70	mA
I _{SB1}	Standby Supply Current (TTL)	CE1 = V _{IH} or CE2 = V _{IL}	-	2	-	2	-	2	mA
I _{SB2}	Standby Supply Current (CMOS)	CE1 = CE2 ≥ V _{DD} - 0.2V or CE2 ≤ 0.2V	-	120	-	150	-	275	µA
I _{DR3}	3.0V Data Retention Supply Current	CE1 = CE2 ≥ V _{DD} - 0.2V or CE2 ≤ 0.2, V _{DD} = 3.0V	-	30	-	60	-	110	µA
I _{DR2}	2.0V Data Retention Supply Current	CE1 = CE2 ≥ V _{DD} - 0.2V or CE2 ≤ 0.2, V _{DD} = 2.0V	-	25	-	50	-	100	µA
V _{OL}	Output Voltage Low	I _{OUT} = 2.1mA	-	0.4	-	0.4	-	0.4	V
V _{OH}	Output Voltage High	I _{OUT} = -1.0mA	2.4	-	2.4	-	2.4	-	V

DATA RETENTION CHARACTERISTICS: Over the operating ranges.					
Symbol	Parameter	Test Condition	Min.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	CE1 = CE2 ≥ V _{DD} - 0.2V or CE2 ≤ 0.2V	2.0	5.5	V
t _{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveforms	0	-	ns
t _r	Operation Recovery Time	See Data Retention Waveforms	t _{rc} *	-	ns

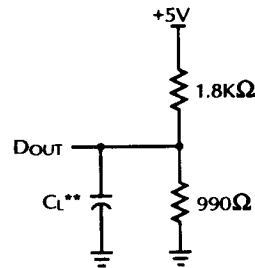
* t_{rc} = Read Cycle Time.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.
 ** Including Probe and Jig Capacitance.

OUTPUT LOAD		
Load	CL	Parameters Measured
1	100 pF	except tCLZ, tCHZ, tOHZ, tOLZ, tWLZ and tWHZ
2	5 pF	tCLZ, tCHZ, tOHZ, tOLZ, tWLZ and tWHZ

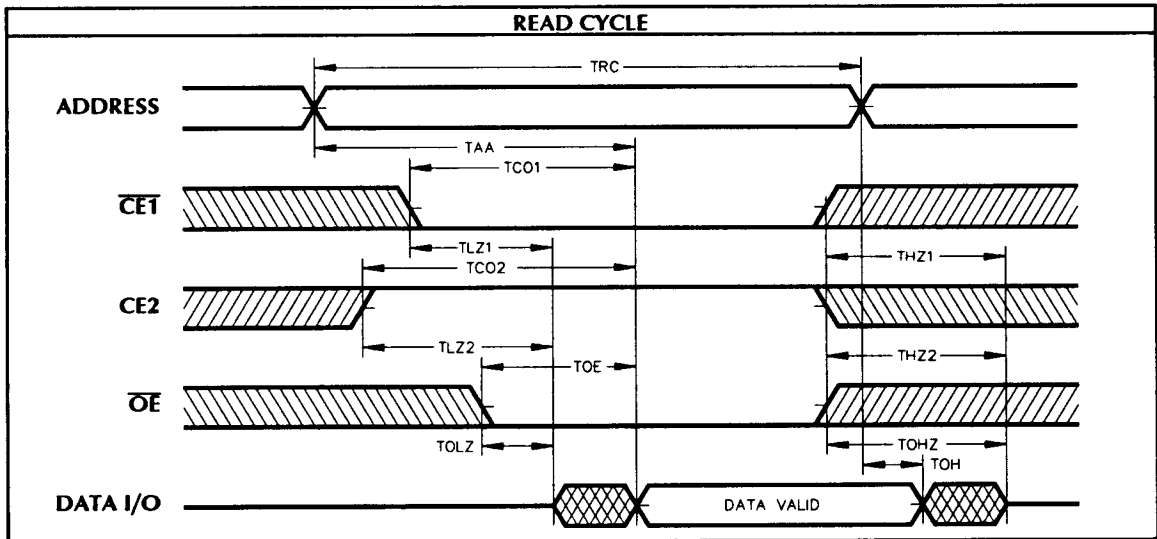
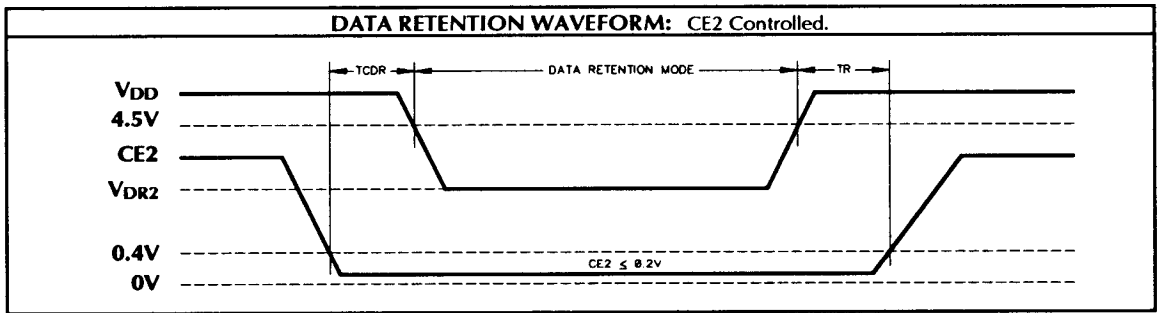
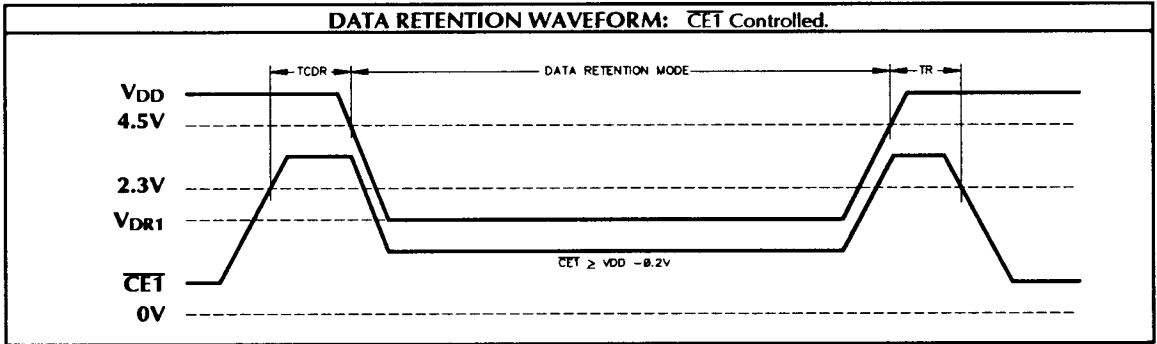
Figure 1. Output Load

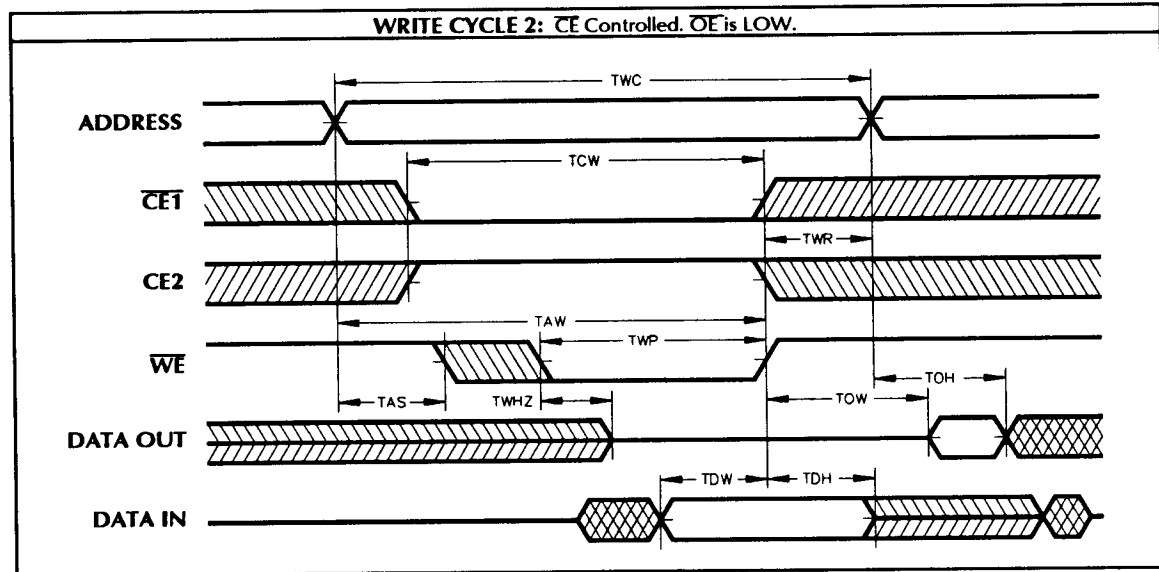
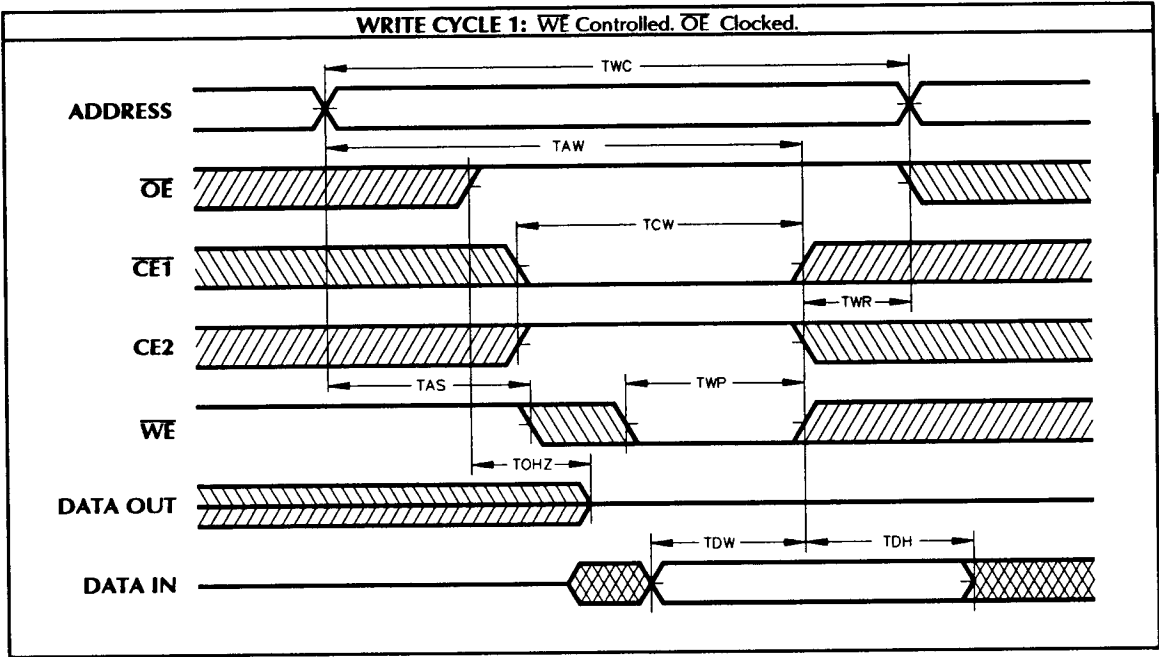


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges 6,7											
No.	Symbol	Parameter	-90†		-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	tRC	Read Cycle Time	90		100		120		150		ns
2	tAA	Address Access Time		90		100		120		150	ns
3	tCO1	Chip Enable (CE1) to Output Valid		90		100		120		150	ns
4	tCO2	Chip Enable (CE2) to Output Valid		90		100		120		150	ns
5	tOE	Output Enable to Output Valid		50		50		60		70	ns
6	tLZ1	Chip Enable (CE1) to Output in LOW-Z 4, 5	10		10		10		10		ns
7	tLZ2	Chip Enable (CE2) to Output in LOW-Z 4, 5	10		10		10		10		ns
8	tOLZ	Output Enable to Output in LOW-Z 4, 5	5		5		5		5		ns
9	tHZ1	Chip Enable (CE1) to Output in HIGH-Z 4, 5		35		35		40		50	ns
10	tHZ2	Chip Enable (CE2) to Output in HIGH-Z 4, 5		35		35		40		50	ns
11	tOHZ	Output Enable to Output in HIGH-Z 4, 5		35		35		40		50	ns
12	tOH	Output Hold from Address Change	10		10		10		10		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges 6,7											
No.	Symbol	Parameter	-90†		-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	tWC	Write Cycle Time	90		100		120		150		ns
14	tCW1	Chip Enable (CE1) to End of Write	75		80		85		90		ns
15	tCW2	Chip Enable (CE2) to End of Write	75		80		85		90		ns
16	tAW	Address Valid to End of Write	75		80		85		90		ns
17	tAS	Address Set-up Time***	0		0		0		0		ns
18	tWP	Write Pulse Width	60		65		70		75		ns
19	tWR	Write Recover Time	0		0		0		0		ns
20	tWHZ	Write Enable to Output in HIGH-Z 4, 5		35		35		40		45	ns
21	tDW	Data to Write Time Overlap	50		50		50		50		ns
22	tDH	Data Hold Time	0		0		0		0		ns
23	tOW	Output Active from End of Write	5		5		5		5		ns

† Commercial Only.
 *** Valid for both Read and Write Cycles.

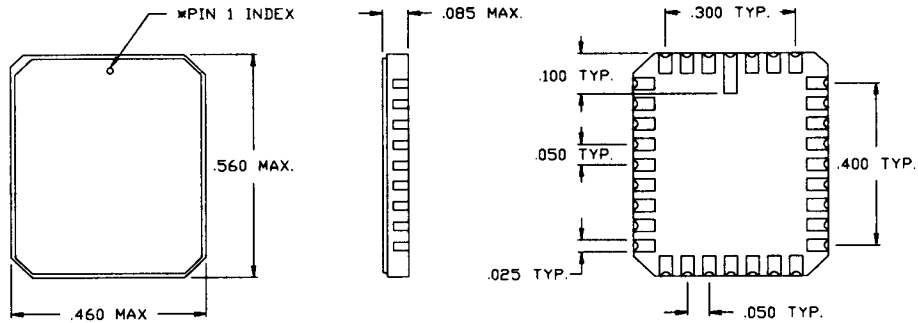




ORDERING INFORMATION

DP	S9264G	-	XX	X			
<u>PREFIX</u>	<u>DEVICE TYPE</u>		<u>SPEED</u>	<u>GRADE</u>	C	COMMERCIAL	0°C to +70°C
					I	INDUSTRIAL	-40°C to +85°C
					M	MILITARY	-55°C to +125°C
					B	MIL-PROCESSED	-55°C to +125°C
					90	90ns	
					10	100ns	
					12	120ns	
					15	150ns	
						8KX8 CMOS SRAM 32-PAD LCC	

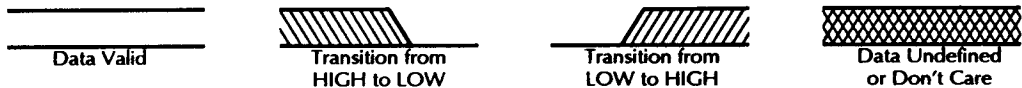
MECHANICAL DIAGRAM



NOTES:

1. All voltages are with respect to V_{SS} .
2. -1.0V min. for pulse width less than 20ns (V_{IL} min. = -0.3V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is sampled and not 100% tested.
5. Transition is measured at the point of $\pm 500mV$ from steady state voltage.
6. When \overline{OE} and \overline{CE} are LOW and \overline{WE} is HIGH, I/O pins are in the output state; and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when \overline{WE} is LOW.

WAVEFORM KEY



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